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EXAMINER	
MANOSKEY, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 07/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,237	VEDAM ET AL.	
	Examiner	Art Unit	
	Joseph D. Manoskey	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/28/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 6, 7, 9-11, 13, 14, 17-20, 22, 23 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Nitschke et al., U.S. Patent 6,463,555, hereinafter referred to as "Nitschke".

3. Referring to claim 1, Nitschke teaches a watchdog circuit that monitors a processor, this is interpreted as a watchdog system for monitoring functionality of a processor (See Col. 1, lines 34-36). Nitschke teaches the watchdog circuit having a comparator circuit that receives a test signal WDS output by the processor, this is interpreted as control logic having N number of acknowledgement signal inputs (See Fig. 1 and Col. 2, lines 17-20). Nitschke discloses having a wide time slot at the starting phase of the program sequence of the processor for the watchdog, this is interpreted as

a first timer, wherein said first timer is started upon boot up of said watchdog system (See Col. 1, lines 34-54). Nitschke teaches a time slot with a beginning and end of time, this is interpreted as second timer and a third timer, wherein said second and third timers are started upon receiving a first acknowledgement signal at one of said N number of acknowledgement signal inputs (See Col. 2, lines 1-19). Finally Nitschke teaches the watchdog circuit generates a reset signal for the processor, this is interpreted as a reset signal generator (See Col. 1, lines 4-9).

4. Referring to claim 2, Nitschke teaches generating a reset signal if the test signal does not appear in a time slot specified by the watchdog circuit and a widened time slot for the starting phase of the program sequence of the processor, this is interpreted as wherein said reset signal generator generates a reset signal upon any one of the following conditions being met: not receiving an acknowledgement signal at one of said N number of acknowledgement signal inputs before an expiration of said first timer (See Col. 1, lines 4-9 and Col. 1, lines 34-54). Nitschke also teaches a time slot with a beginning and end and generating a signal if lower and upper threshold are not met, this is interpreted as receiving an acknowledgement signal at one of said N number of acknowledgement signal inputs before an expiration of said second timer and not receiving an acknowledgement signal at all of said N number of acknowledgement signal inputs before an expiration of said third timer (See Col. 2, lines 1-20).

5. Referring to claim 3, Nitschke discloses the comparator circuit connected to the test signal WDS output by the processor, this is interpreted as further comprising an interface coupled to said control logic via said N number of acknowledgement signal inputs, wherein said interface couples said processor to said watchdog system (See Fig. 1 and Col. 2, lines 17-20).

6. Referring to claim 4, Nitschke teaches the comparator circuit outputs a rest signal to the processor, this is interpreted as wherein said reset signal resets said processor coupled to said processor interface (See Fig. 1 and Col. 2, lines 30-33).

7. Referring to claim 6, Nitschke teaches shifting the values of either the upper or lower value of the time slot, this is interpreted as wherein a duration of each said timers can be set to unique values (See Col. 2, lines 59-62).

8. Referring to claim 7, Nitschke discloses test signal being output by the processor, this is interpreted as wherein said N number of acknowledgement signal inputs are input/output lines (See Col. 2, lines 19-21).

9. Referring to claim 9, Nitschke teaches a watchdog circuit that monitors a processor, this is interpreted as a method of monitoring functionality of a processor (See Col. 1, lines 34-36). Nitschke teaches a time slot with a beginning and end of time, this is interpreted as starting a first timer and starting a second timer (See Col. 2, lines 1-

19). Nitschke teaches the watchdog circuit having a comparator circuit that receives a test signal WDS output by the processor, this is interpreted as receiving at least one acknowledgement signal from a processor or software module (See Fig. 1 and Col. 2, lines 17-20). Nitschke teaches when the test signal WDS is received correctly a reset signal is sent to the clock counter, this is interpreted as upon the reception of every one of at least one acknowledgement signal, restarting said first timer (See Col. 2, lines 42-44). Nitschke teaches a time slot with a beginning and end of time, this is interpreted as resetting said processor if any one of the following conditions are met: receiving any one of said at least one acknowledgement signal prior to an expiration of said first timer and not receiving all of said at least one acknowledgement signal prior to an expiration of said second timer (See Col. 2, lines 1-41).

10. Referring to claim 10, Nitschke also teaches a time slot with a beginning and end and generating a signal if lower and upper threshold are not met, this is interpreted as wherein said first and second timers are started simultaneously (See Col. 2, lines 1-20).

11. Referring to claim 11, Nitschke discloses having a wide time slot at the starting phase of the program sequence of the processor for the watchdog and once the starting phase has finished the time slot is returned to its original width, this is interpreted as further comprising the step of receiving a signal indicating that said processor is properly initialized, wherein said first and second timers are started upon receiving said initialization signal (See Col. 1, lines 34-54).

12. Referring to claim 13, Nitschke discloses a have a wide time slot at the starting phase of the program sequence of the processor for the watchdog, this is interpreted as starting a boot up timer (See Col. 1, lines 34-54). Nitschke also teaches generating a reset signal if the test signal does not appear in a time slot specified by the watchdog circuit and a widened time slot for the starting phase of the program sequence of the processor, this is interpreted as resetting said processor if an initialization signal is not received from said processor prior to an expiration of said boot up timer, wherein said initialization signal indicates that said processor is properly initialized (See Col. 1, lines 4-9 and Col. 1, lines 34-54).

13. Referring to claim 14, Nitschke also teaches a time slot with a beginning and end and generating a signal if lower and upper threshold are not met, this is interpreted as wherein said first and second timers are simultaneously started upon receiving said initialization signal (See Col. 2, lines 1-20).

14. Referring to claim 17, Nitschke teaches a watchdog circuit that monitors a processor, this is interpreted as a watchdog system for monitoring functionality of a processor (See Col. 1, lines 34-36). Nitschke teaches the watchdog circuit having a comparator circuit that receives a test signal WDS output by the processor, this is interpreted as control logic having N number of acknowledgement signal inputs (See Fig. 1 and Col. 2, lines 17-20). Nitschke discloses having a wide time slot at the starting

phase of the program sequence of the processor for the watchdog, this is interpreted as a boot up timer, wherein said boot up timer is started at the start of a boot up of a processor (See Col. 1, lines 34-54). Nitschke teaches a time slot with a beginning and end of time, this is interpreted as a forbidden timer, wherein the said forbidden timer is started upon start of every operational cycle after completion of a successful boot up of said processor, an acknowledgement timer, wherein said acknowledgement timer is started upon receiving an acknowledgement signal at one of said N number of acknowledgement signal inputs and a cycle period timer, wherein said cycle period timer is started upon start of every operational cycle after completion of a successful boot up of said processor (See Col. 2, lines 1-19). Finally Nitschke teaches the watchdog circuit generates a reset signal for the processor, this is interpreted as a reset signal generator (See Col. 1, lines 4-9).

15. Referring to claim 18, Nitschke teaches generating a reset signal if the test signal does not appear in a time slot specified by the watchdog circuit and a widened time slot for the starting phase of the program sequence of the processor, this is interpreted as wherein said reset signal generator generates a reset signal to said processor upon any one of the following conditions being met: not receiving an acknowledgement signal at a first one of said N number of acknowledgement signal inputs before an expiration of said boot up timer (See Col. 1, lines 4-9 and Col. 1, lines 34-54). Nitschke also teaches a time slot with a beginning and end and generating a signal if lower and upper threshold are not met, this is interpreted as receiving an acknowledgement signal at any

one of said N number of acknowledgement signal inputs before an expiration of said acknowledgement, receiving an acknowledgement signal at any one of said N number of acknowledgement signal inputs before an expiration of said forbidden timer and not receiving an acknowledgement signal at all of said N number of acknowledgement signal inputs before an expiration of said cycle period timer (See Col. 2, lines 1-20).

16. Referring to claim 19, Nitschke discloses the comparator circuit connected to the test signal WDS output by the processor, this is interpreted as further comprising an interface coupled to said control logic via said N number of acknowledgement signal inputs, wherein said interface couples said processor to said watchdog system (See Fig. 1 and Col. 2, lines 17-20).

17. Referring to claim 20, Nitschke teaches the comparator circuit outputs a rest signal to the processor, this is interpreted as wherein said reset signal resets said processor coupled to said processor interface (See Fig. 1 and Col. 2, lines 30-33).

18. Referring to claim 22, Nitschke teaches shifting the values of either the upper or lower value of the time slot, this is interpreted as wherein a duration of each said timers can be set to unique values (See Col. 2, lines 59-62).

19. Referring to claim 23, Nitschke discloses test signal being output by the processor, this is interpreted as wherein said N number of acknowledgement signal inputs are input/output lines (See Col. 2, lines 19-21).

20. Referring to claim 25, Nitschke teaches a watchdog circuit that monitors a processor, this is interpreted as a method of monitoring the functionality of a processor (See Col. 1, lines 34-36). Nitschke discloses having a wide time slot at the starting phase of the program sequence of the processor for the watchdog, this is interpreted as starting a boot up timer (See Col. 1, lines 34-54). Nitschke teaches a time slot with a beginning and end of time, this is interpreted as starting a forbidden timer, starting a cycle period timer (See Col. 2, lines 1-19). Nitschke teaches the watchdog circuit having a comparator circuit that receives a test signal WDS output by the processor, this is interpreted as receiving at least one acknowledgement signal, upon the reception of one of at least one acknowledgement signal, starting an acknowledgement timer (See Fig. 1 and Col. 2, lines 17-20).

Nitschke teaches generating a reset signal if the test signal does not appear in a time slot specified by the watchdog circuit and a widened time slot for the starting phase of the program sequence of the processor, this is interpreted as wherein said reset signal generator generates a reset signal to said processor upon any one of the following conditions being met: not receiving an acknowledgement signal at a first one of said N number of acknowledgement signal inputs before an expiration of said boot up timer (See Col. 1, lines 4-9 and Col. 1, lines 34-54). Nitschke also teaches a time slot

with a beginning and end and generating a signal if lower and upper threshold are not met, this is interpreted as receiving an acknowledgement signal at any one of said N number of acknowledgement signal inputs before an expiration of said acknowledgement, receiving an acknowledgement signal at any one of said N number of acknowledgement signal inputs before an expiration of said forbidden timer and not receiving an acknowledgement signal at all of said N number of acknowledgement signal inputs before an expiration of said cycle period timer (See Col. 2, lines 1-20).

21. Claims 15 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Cahill, U.S. Patent Application Publication 2003/0204792, hereinafter referred to as "Cahill".

22. Referring to claim 15, Cahill teaches a watchdog timers system that issues an interrupt and upon the interrupt being generated the current processor state is saved and an interrupt handler executes that resets the system, this is interpreted as a method of resetting a processor coupled to watchdog comprises the steps of monitoring a processor using a watchdog coupled to said processor, resetting said processor using said watchdog, storing state information of said processor immediately prior to resetting said processor, wherein said state information indicates a state the processor was in prior to reset (See Page 6, paragraphs 0054 and 0055).

23. Referring to claim 16, Cahill teaches the interrupts can be non-maskable interrupts, this is interpreted as wherein said step of storing comprises the step of asserting a non-maskable interrupt (See Page 4, paragraph 0035).

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claims 5, 12, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nitschke in view of Cahill.

26. Referring to claim 5, Nitschke teaches all the limitations (See rejection of claim 4) except for further includes logic to save information pertaining to a state of said processor immediately prior to reset. Cahill teaches a watchdog timers system that issues an interrupt and upon the interrupt being generated the current processor state is saved and an interrupt handler executes that resets the system (See Cahill, Page 6, paragraphs 0054 and 0055). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the watchdog Nitschke with saving the processor state of Cahill. This would have been obvious to one of ordinary skill in the

art at the time of the invention to do because provides suitable error handling and recovery (See Cahill, Page 6, paragraph 0054).

27. Referring to claim 12, Nitschke teaches all the limitations (See rejection of claim 9) except for wherein said step of resetting said processor further comprises the step of storing state information pertaining to said processor. Cahill teaches a watchdog timers system that issues an interrupt and upon the interrupt being generated the current processor state is saved and an interrupt handler executes that resets the system (See Cahill, Page 6, paragraphs 0054 and 0055). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the watchdog Nitschke with saving the processor state of Cahill. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because provides suitable error handling and recovery (See Cahill, Page 6, paragraph 0054).

28. Referring to claim 21, Nitschke teaches all the limitations (See rejection of claim 20) except for further includes logic to save information pertaining to a state of said processor immediately prior to reset. Cahill teaches a watchdog timers system that issues an interrupt and upon the interrupt being generated the current processor state is saved and an interrupt handler executes that resets the system (See Cahill, Page 6, paragraphs 0054 and 0055). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the watchdog Nitschke with saving the processor state of Cahill. This would have been obvious to one of ordinary skill in the

art at the time of the invention to do because provides suitable error handling and recovery (See Cahill, Page 6, paragraph 0054).

29. Claim 8 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nitschke is view of Shieh et al., U.S. Patent 6,377,851, hereinafter referred to as "Shieh".

30. Referring to claim 8, Nitschke teaches all the limitations (See rejection of claim 1) except wherein said N number of acknowledgement signal inputs are registers. Nitschke does discloses test signal being output by the processor but is silent on whether the signal is from a register (See Nitschke, Col. 2, lines 19-21). Shieh teaches a watchdog system and acknowledging by using registers (See Shieh, Col. 7, lines 9-18). It would have been obvious to one of ordinary skill in the art at the time of the invention combine the watchdog signals of Nitschke with the registers of Shieh. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because the registers allow various software processes to change the hardware configuration (Shieh, Col. 7, lines 9-18).

31. Referring to claim 24, Nitschke teaches all the limitations (See rejection of claim 17) except wherein said N number of acknowledgement signal inputs are registers. Nitschke does discloses test signal being output by the processor but is silent on whether the signal is from a register (See Nitschke, Col. 2, lines 19-21). Shieh teaches

a watchdog system and acknowledging by using registers (See Shieh, Col. 7, lines 9-18). It would have been obvious to one of ordinary skill in the art at the time of the invention combine the watchdog signals of Nitschke with the registers of Shieh. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because the registers allow various software processes to change the hardware configuration (Shieh, Col. 7, lines 9-18).

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following are closely related watchdog systems.

U.S. Patent 4,832,594 to Youtz

U.S. Patent 5,694,336 to Hirao

U.S. Patent 6,675,320 to Schumacher et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Manoskey whose telephone number is (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JDM
July 17, 2006

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